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	Filing Date	2000-01-21
	First Named Inventor	Paul W. SHERER
	Art Unit	2152
	Examiner Name	Aaron N. STRANGE
	Attorney Docket Number	1112.US.CIP

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	1	NATIONAL SEMICONDUCTOR, NS 16550A Universal Asynchronous Receiver/Transmitter with FIFOs, 1988.	<input type="checkbox"/>
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	3	FUJITSU, LTD, Data sheet for "FUJITSU MB86950 Etherstar Ethernet Controller", December 1989.	<input type="checkbox"/>
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5	FRAZIER, GREGORY L and YUVAL TARIAR, "The Design and Implementation of a Multi-Queue Buffer for VLSI Communication Switches", IEEE, 1989.	<input type="checkbox"/>
6	INTEL, CORP, Datasheet for 82596CA High-Performance 32-Bit Local Area Network Coprocessor", November 1989.	<input type="checkbox"/>
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11	NATIONAL SEMICONDUCTOR, Data sheet for "DP 83265 BSI Device (FDDI System Interface)", February 1991.	<input type="checkbox"/>
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16	MOTOROLA, "FDDI System Interface Users Manual, MC68639", 1994.	<input type="checkbox"/>
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